We claim:

1. A method for producing micromachined devices, comprising the steps of:

   (a) obtaining a Silicon-On-Insulator (SOI) wafer, which comprises

      (i) a handle layer,

      (ii) a dielectric layer, and

      (iii) a device layer;

      wherein a mesa etch has been made on the device layer of the SOI wafer,

   (b) obtaining a substrate, wherein a pattern has been formed onto the substrate;

   (c) bonding the SOI wafer and the substrate together;

   (d) removing the handle layer of the SOI wafer;

   (e) removing the dielectric layer of the SOI wafer; and

   (f) performing a structural etch on the device layer.

2. The method of claim 1, wherein the dielectric layer of the SOI wafer comprises silicon dioxide.

3. The method of claim 1, wherein the structural etch is a Deep Reactive Ion Etch.

4. The method of claim 1, wherein the substrate comprises at least one access port.

5. The method of claim 1, wherein the substrate is glass or silicon.

6. The method of claim 1, wherein the substrate is glass and the substrate pattern comprises multilevel metallization.

7. The method of claim 1, wherein the substrate is a recess-etched glass wafer.

8. The method of claim 7, further comprising the steps of

   (a) performing a blanket sputter of the multilevel metallization; and

   (b) lifting off the metal not directly applied to the substrate.

9. The method of claim 1, wherein the bonding of the SOI wafer and the substrate is anodic bonding.

10. The method of claim 1, wherein removing the handle layer of the SOI wafer comprises removing the handle layer of the SOI wafer by a wet chemical etch.

11. The method of claim 1, wherein removing the dielectric layer of the SOI wafer comprises removing the dielectric layer of the SOI wafer by a dry plasma etch.

12. The method of claim 1, wherein said substrate comprises an SOI wafer.

13. The method of claim 1, wherein the structural etch is straight down through the device layer to the substrate.

14. The method of claim 13, wherein the device layer is partially removed at the top surface at locus where the structural etch is to be performed straight down to the substrate, such that when the device layer is bonded to the substrate, the surface of the device layer at the locus is spaced apart from the substrate.

15. The method of claim 1, wherein said substrate includes a patterned metal layer deposited thereon, wherein the metal layer defines gaps, which are positioned other than under operable elements which is to be formed by etching the device layer.

16. The method of claim 1, wherein bonding the SOI wafer and the substrate together is performed under a predetermined pressure less than atmosphere pressure.

17. The method of claim 1, wherein removing the handle layer of the SOI wafer comprises:

(a). removing the handle layer of the SOI wafer to a predetermined distance from the dielectric layer by a first etchant, wherein a relatively thin handle layer is left on the dielectric layer; and

(b). removing the relatively thin handle layer by a second etchant.

18. The method of claim 17, wherein said first etchant is a relatively fast etchant.

19. The method of claim 17, wherein said second etchant is a relatively slow etchant.

20. The method of claim 17, wherein said first etchant is potassium hydroxide (KOH).

21. The method of claim 17, wherein said second etchant is xenon difluoride (XeF_2).

22. The method of claim 17, wherein said second etchant is tetramethyl ammonium hydroxide (TMAH).

23. A method for making an accelerometer, comprising the steps of:

(a) obtaining a Silicon-On-Insulator (SOI) wafer, which comprises

(i) a handle layer,

(ii) a dielectric layer, and

(iii) a device layer;

wherein a mesa etch has been made on the device layer of the SOI wafer;

(b) obtaining a substrate, wherein a pattern has been formed onto the substrate;

(c) bonding the SOI wafer and the substrate together;

(d) removing the handle layer of the SOI wafer;

(e) removing the dielectric layer of the SOI wafer; and

(f) performing a structural etch on the device layer, such that the etches of the mesa etch and the structural etch provide a pattern for an accelerometer.

24. A method for producing micromachined devices, comprising the steps of:

(a) obtaining a Silicon-On-Insulator (SOI) wafer, which comprises

(i) a handle layer,

(ii) a dielectric layer, and

(iii) a device layer;

wherein a mesa etch has been made on the device layer of the SOI wafer, and a structural etch has been made in the device layer of the SOI wafer,

(b) obtaining a substrate, wherein a pattern has been formed onto the substrate;

(c) bonding the SOI wafer and the substrate together under a predetermined pressure less than atmosphere pressure;

(d) removing the handle layer of the SOI wafer; and

(e) removing the dielectric layer of the SOI wafer.

25. A method for producing micromachined devices, comprising the steps of:

(a) obtaining a Silicon-On-Insulator (SOI) wafer, which comprises

(i) a handle layer,

(ii) a dielectric layer, and

(iii) a device layer;

wherein a mesa etch has been made on the device layer of the SOI wafer, and a structural etch has been made in the device layer of the SOI wafer,

(b) obtaining a substrate, wherein a pattern has been formed onto the substrate;

(c) bonding the SOI wafer and the substrate together;

(d) removing the handle layer of the SOI wafer to a predetermined distance from the dielectric layer by a first etchant, wherein a relatively thin handle layer is left on the dielectric layer;

(e) removing the relatively thin handle layer by a second etchant; and

(f) removing the dielectric layer of the SOI wafer.

26. The method of claim 25, wherein said first etchant is a relatively fast etchant.

27. The method of claim 25, wherein said second etchant is a relatively slow etchant.

28. The method of claim 25, wherein said first etchant is potassium hydroxide (KOH).

29. The method of claim 25, wherein said second etchant is xenon difluoride (XeF_2).

30. The method of claim 25, wherein said second etchant is tetramethyl ammonium hydroxide (TMAH).

31. A structure with a substrate for etching with dry plasma etch having an element overlying and spaced apart from said substrate, comprising a metal layer deposited on said substrate, wherein said metal layer is substantially uniform under said element, wherein said metal layer includes one or more gaps in said metal layer, wherein said gaps are positioned other than under said element.